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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/706,029	11/13/2003	Visvesvaraya A. Pentakota	TI-37058	6199
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TEXAS INSTRUMENTS INCORPORATED P O BOX 655474, M/S 3999 DALLAS, TX 75265			EXAMINER LAUTURE, JOSEPH J	
			ART UNIT	PAPER NUMBER
			2819	

DATE MAILED: 11/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

**Application No.**

10/706,029

**Applicant(s)**

PENTAKOTA, VISVESVARAYA A.

**Examiner**

Joseph Lauture

**Art Unit**

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 13 November 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-5, 11 and 17-20 is/are rejected.
- 7) ☒ Claim(s) 6-10, 12-16 and 18-20 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 13 November 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## **DETAILED ACTION**

### *Specification*

The application has not been checked to the extent necessary to determine the presence of all possible typographical and grammatical errors. Applicant's cooperation is requested in correcting any errors of which he/she may become aware in the application.

### ***Claim Rejections - 35 USC § 112***

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-4 and 17-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1 and 17 recite on lines 6 and 7 the limitation "if said desired voltage were to be applied at said first node". This limitation is unclear and confusing because as shown in figure (2b), the desired voltage produced by the voltage source (290) is indeed coupled to the node (212).

Claims 2-4 and 18-20 are also rejected under 35 U.S.C 112 2<sup>nd</sup> paragraph since they depend on independent claims 1 and 17 which have been rejected under 35 U.S.C 112, 2<sup>nd</sup> paragraph.

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

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A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 1 is rejected under 35 U.S.C 102(b) as being anticipated by Janssen et al (US 6,384,817).

Janssen et al teach in figure (2) an apparatus for applying a desired voltage at a node, the node being connected to a load impedance ( $Z_i$ ), said apparatus comprising a voltage source (22) coupled to the node, the voltage source (22) generating said desired voltage; and, a current source ( $I_{comp}$ ) also coupled to the node, wherein said current source draws a current that is approximately equal to the current across the load impedance, since the current ( $I_{col}$ ) flowing through the load impedance ( $Z_i$ ) (See column 5, lines 23-25) equals the current ( $I_{comp}$ ) drawn by the current source, to avoid voltage transients (See column 5, lines 29-31).

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 5, 11 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Caruso et al (US 5,592,167) in view of Rivoir et al (US 5,703,588) and Janssen et al (US 6,384,817).

Regarding claims 5 and 11, Caruso et al teaches in figure (5A) an analog-to-digital converter for converting an analog signal to a digital code, the converter

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comprising a plurality of stages (See figure 8), each of said plurality of stages generating a corresponding one of a plurality of sub-codes used to generate said digital code, each of said plurality of stages comprising as shown in figure 5A: an analog-to-digital converter, a resistor ladder having a first end and a second end, said first end of the resistor ladder being connected to a current source (46), said current source supplying to said resistor ladder an amount of current producing desired voltages across the resistors of the ladder.

Caruso et al teach the essential features of the claimed invention as set forth above except for a voltage source connected to the resistor ladder. However, Rivoir et al teach in figure (6) a digital-to-analog converter apparatus including a voltage source and a current source (54) both connected to a resistor ladder to control current distribution in the system. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Rivoir et al into the system of Caruso et al to improve system performance and reliability because this would reduce linearity errors in the system (See column 6, lines 25-28). It would have been further obvious to provide additional circuitry to refine the digital codes obtained as required by a given application.

Regarding claim 17, Janssen teach the essential features of the claimed invention as set forth above, except that the claimed invention is implemented on an integrated circuit chip. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to carry out the invention in the form of an I.C

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chip because this would broaden the range of applications of the invention by reducing space requirement in a system.

***Allowable Subject Matter***

Claims 6-10, 12-16 and 18-20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

**Reasons For Indication of Allowable Subject Matter**

The following is a statement of reasons for the indication of allowable subject matter: the prior arts of record fail to teach an apparatus for applying a desired voltage to a given node in a circuit, the apparatus comprising in each of a plurality of stages a current source and a voltage source both coupled to a load impedance, wherein said current source enables the voltage source to be coupled to the node without a buffer between the voltage source and the node, and wherein each stage further comprises an analog-to-digital converter and a digital-to-analog converter, a subtractor and an amplifier the output of the subtractor.

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### CONTACT INFORMATION

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph Lauture, whose telephone number is (571) 272-1805. The examiner can normally be reached Monday thru Friday between 9:30 am and 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Tokar can be reached at (571) 272-1812. The fax number for the organization to which this application is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the group receptionist whose telephone number is (571) 272-1562.

Joseph Lauture  
Group: 2819  
Date: 10/29/2004

  
Michael Tokar  
Supervisory Patent Examiner  
Technology Center 2800